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10/019,059	04/19/2002	Damian Dalton	006838-079	8679

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/019,059	DALTON, DAMIAN	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/23/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 have been presented for examination based on the application filed on 19th April 2002.
2. Claims 19-35 disclosed in the preliminary amendment submitted on 27th December 2001 were not presented for examination, as there was no markup set present for those claims.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. S990535 (& PCT/IE00/00083) filed on 06/28/1999 (06/28/2000).

Specification

4. This application does not contain an abstract of the disclosure as required by 37 CFR 1.72(b). An abstract on a separate sheet is required.
5. A substitute specification including the claims is required pursuant to 37 CFR 1.125(a) because multiple specifications as part of the various NPL documents and foreign applications was submitted not complying with suggested format for the specification.

   A substitute specification must not contain new matter. The substitute specification must be submitted with markings showing all the changes relative to the immediate prior version of the specification of record. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before

and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strike-through cannot be easily perceived. An accompanying clean version (without markings) and a statement that the substitute specification contains no new matter must also be supplied. Numbering the paragraphs of the specification of record is not considered a change that must be shown.

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) The Names Of The Parties To A Joint Research Agreement: See 37 CFR 1.71(g).

(e) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and

including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(g) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(h) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(i) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(j) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(k) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(l) Sequence Listing. See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Logic Event Simulation Using Content Addressable Memory".

Claim Objections

7. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim, which depends from a dependent claim, should not be separated by any claim, which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Claims 6 and 8-9 depend improperly from claims 4 and 3 respectively.

8. Further claims 2 & 4 have grammatical errors. Claim 2 last step is not grammatically correct. Claim 4 (from preliminary amendment) has spelling error "ha". Appropriate corrections are required.

Drawings

9. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because drawings presented are not properly legible due to over saturation and are turned in as part of foreign application and not specification for instant application. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112 ¶2nd

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

9. Claim 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1

Claim 1 discloses a method but the steps defined in the method do not perform a function, instead it describes the supposed hardware mechanism for evaluation. The preamble of the claims seems to be reciting the steps of the method, but cannot be given same patentable weight as the steps of the method. As presented the claim 1 does not clearly recite a method that a person skilled in the art would be able to use/make the present invention. Examiner respectfully suggests rewriting the present claim to appropriately recite the method steps of the current invention.

Regarding Claim 2

Claim 2 last-step discloses, "count continues until the remainder represents the count still required". Examiner is unclear what limitation this step is representing as the grammatical error has rendered this claim beyond reasonable comprehension.

Regarding Claim 3-15

Claims 3-15 are rejected based on their dependency on the parent claim 1.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> **Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.**

10. Claims 1-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Although the claim 1 discloses association with hardware mechanism (associative memory mechanism) it does not disclose any tangible medium. Claim 1 is non-statutory, as a human being could manually perform the steps defined in the method above. MPEP 2111 states:

> **In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (Claim 9 was directed to a process of analyzing data generated by mass spectrographic analysis of a gas. The process comprised selecting the data to be analyzed by subjecting the data to a mathematical manipulation. The examiner made rejections under 35 U.S.C. 101 and 102. In the 35 U.S.C. 102 rejection, the examiner explained that the claim was anticipated by a mental process augmented by pencil and paper markings. The court agreed that the claim was not limited to using a machine to carry out the process since the claim did not explicitly set forth the machine. The court explained that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim,' to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The court found that applicant was advocating the latter, i.e., the impermissible importation of subject matter from the specification into the claim.)**

There is no tangible medium recited in the claimed method to bring the method into the technological art. Examiner respectfully suggests following language for the preamble "A Computer implemented parallel processing method for controlling [...]".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1 and 3-18 are rejected under 35 U.S.C. 102(b) as being anticipated by CompEuro '92 Article "An associative memory approach to parallel logic event-driven simulation" by Damian Dalton (Dalton1992 hereafter).

Regarding Claim 1

Dalton1992 teaches a parallel processing method (Dalton1992: Fig.1) of logic simulating comprising representing signals on a line over a time period as a bit sequence, evaluating the output of any Logic gate including an evaluation of any inherent delay by a comparison between the bit sequences of the inputs of the Logic gate to a predetermined series of bit patterns and in which those Logic gates whose outputs have changed over the time period are identified during the evaluation of the gate outputs as real gate changes and only those real gate changes are propagated to the fan out gates of those Logic gates (Dalton1992: Pg.341 Introduction; Pg.342 Bit sequence representation; Pg.342 (vi), (viii)); characterized in that the control of the method is carried out in an associative memory mechanism (1a, 1b) which stores in word form a history of gate input signals by compiling a hit-list register (Dalton1992: Pg.345, Col.1 ¶2) of logic gate state changes and using a multiple response revolver (C) forming part of the associative memory mechanism (1a, 1b)

which generates an address for each hit and then scans and transfers the results on the hit list to an output register for subsequent use (Dalton1992: The Apples System; Fig.6).

Regarding Claim 3

Dalton1992 teaches the hit list is segmented into a plurality of separate smaller hit-lists (Dalton1992: Pg.345, Col.1 ¶2), each connected to a separate scan register and in which each scan register is operated in parallel to transfer the results to the output register the hit list is segmented into a plurality of separate smaller hit lists, each connected to a separate scan register and in which each scan register is operated in parallel to transfer the results to the output register (Dalton1992: Pg.345-346, evaluation procedure – "Begin...test size register.. End" section).

Regarding Claim 4

Dalton1992 teaches associative register divided into separate smaller associative sub-registers, one type of logic gate being allocated to each associative sub-register, each of which associative sub-register has a corresponding sub-registers connected thereto whereby gate evaluation and tests are carried out in parallel on each associative sub-register (Dalton1992: Fig.6 (Element 1a & 1b); sub-register 1a denoting a gate type; 345-346, evaluation procedure – "Begin...test size register.. End" section; Col.2 – "Result-Activator-register").

Regarding Claim 5

Dalton1992 teaches a method in which each line signal to a target logic gate is stored as a plurality of bits each representing a delay of one time period, the

aggregate bits representing the delay between signal output to and reception by the target logic gate and in which the inherent delay of each logic gate is represented in the same manner (Dalton1992: Pg 341-343 – "m unit inertial delay model"; Fig.2-3).

Regarding Claim 6

Dalton1992 teaches each associative sub-register is used to form a hit list connected to a corresponding separate scan register as "group target hit list" (Dalton1992: Pg.345- Col.2).

Regarding Claim 7

Dalton1992 teaches that where the number of one type of logic gate exceeds a predetermined number more than one sub-register is used (Dalton1992: Fig.6- showing more than one sub-registers).

Regarding Claim 8

Dalton1992 inherently teaches that the scan registers are controlled by exception logic using an d OR gate whereby the scan is terminated for each register on the OR changing state then indicating no further match (Dalton1992: Pg.345, Col.1 ¶3; Fig.6).

Regarding Claim 9

Dalton1992 teaches sequentially clearing the hit list and repeating the clearing process inherently (Dalton1992: Pg.345, Col.1 ¶3).

Regarding Claim 10

Dalton1992 teaches each line signal to a target logic gate is stored as a plurality of bits each representing a delay of one time period, the aggregate bits representing

the delay between signal output to and reception by the target logic gate (Dalton1992: Pg.343 – Bit sequence representation Fig.2-3).

Regarding Claim 11

Dalton1992 teaches an initialization phase where specified signals are inputted (Dalton1992: Pg.343, Test1); unspecified signals are set to unknown or don't cares (Dalton1992: Pg.343, Test2); test templates are prepared defining the delay model of each logic gate (Dalton1992: Pg.342 – bit sequence representation (ii)); input circuit is parsed to generate two-input logic gates (Dalton1992: Pg.342, Col.1 (i)); two level logic gates are then configured (Dalton1992: Pg.342, Col.1 (ii)).

Regarding Claim 12-13

Dalton1992 teaches multi-valued logic is applied and in which n bits are used to represent a signed value at any instance in time with n being any arbitrarily chosen logic (Dalton1992: Pg.342 Col.2 (v)); 8 values logic can also be represented as taught.

Regarding Claim 14

Dalton1992 teaches sequence of values on a logic gate is stored as a bit pattern forming a unique word in the associative memory mechanism (1a, 1b) (Dalton1992: Pg.345, Col.2 ¶1).

Regarding Claim 15

Dalton1992 teaches associative memory storing a record of all values that a logic gate has acquired for the units of delay of the longest delay in the circuit as associative array (1b) storing a record of all values that the logic gate has aquired in

each time step with the farthest one indicating the longest delay (Dalton1992: Pg.342 Col2 – Pg.343 Col.2; Fig.2-4).

Regarding Claim 16

Apparatus/Processor claim 16 discloses similar limitations as claim 1 is rejected for the same reasons as claim 1 (Dalton1992: Fig.6).

Regarding Claim 17

Dalton1992 teaches sub-registers as input sub-register, mask sub-register and scan sub-register (Dalton1992: Fig.5).

Regarding Claim 18

Dalton1992 teaches that scan sub-register are connected to an output register (Dalton1992: Pg.345, Col.1 ¶3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE/ CompEuro '92 Article "An associative memory approach to parallel logic event-driven simulation" by Damian Dalton (Dalton1992 hereafter), in view of IEEE article "Model of auto associative memory that stores and retrieves data regardless of their orthogonality, randomness or size" by Bairaktaris, D. (Bairaktaris hereafter).

Regarding Claim 2

Teachings of Dalton1992 are disclosed in claim 1 rejection above.

Dalton1992 does not explicitly teach delay word exceeding the associative register (1b) and storing the gate state in the state register (1a) but provides the identical implementation of the structure of the associative memory as disclosed in the application. Also Dalton1992 teaches variable lengths and types of delays that can be stored in the CAM (Dalton1992: Pg.345 Col.2, ¶1, Lines 5-7).

Bairaktaris teaches storing information in content associative memory where the size of the stored information is greater than the size of the register and illustrates how state register information calculated, until the information is broken down into content-associative-memory-register's size (Bairaktaris: Pg.143-144, Section 3.5, 4.1).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Bairaktaris to Dalton1992 to divide the delay information if it exceeds the associative register word width. The motivation to combine would have been that Bairaktaris teaches creating auto

associative content addressable memory (CAM) where the size to be stored is greater than the size of the register (Bairaktaris: Introduction). Further, Bairaktaris teaches CAM to be shared CAM (Bairaktaris: Introduction) which Dalton1992 uses to implement the CAM accessed by multiple processors (Dalton1992: Fig.1 Pg.354 Apples system – parallel operations). Similar prior art addressing the overflow in the CAM was also available at the time of instant application[1].

[1] U.S. Patent Nos. 5423015, 6226710.

Conclusion

13. All claims are rejected.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
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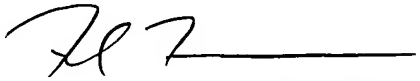
Tuesday, October 25, 2005



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